METHOD OF AUTOMATIC FAULT ISOLATION IN A PROGRAMMABLE LOGIC DEVICE

ABSTRACT

The configuration of a faulty line segment in a switch matrix of a programmable logic device is identified using read-back capture. Each original programmable interconnection point ("PIP") in the line segment is tested by generating routes from a first logic port through the original line segment and PIP, through all PIPs, adjacent to the original PIP to the opposite logic port. Routes through all PIPs adjacent to the PIPs in the line segment from the first logic port to the second logic port, and from the second logic port to the first logic port, are tested to isolate the fault in the line segment.